

### **Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

### **Listing of Claims:**

1. *(Currently Amended)*            A frequency divider comprising,  
   a first latch comprising a clock input for receiving a clock signal, and  
   a second latch comprising a latch circuit configured as a low-pass filter,  
the second latch being crossed-coupled to the first latch;  
   wherein the second latch comprises  
   a differential pair of transistors including  
   a first pair of transistors comprising a first transistor coupled to second  
transistor  
   - a second pair of transistors comprising a third transistor coupled to a  
   fourth transistor  
   - each transistor having a drain, a source and a gate,  
   a drain of the first transistor and a drain of the third transistor being  
coupled to a source of the second transistor and to a source of the fourth transistor  
respectively  
   gates of the second transistor and fourth transistor receiving a signal  
generated by the first latch  
   gates of the first transistor and the third transistor being coupled to a  
control signal for determining a low-pass characteristic of the second latch.

2. *(Canceled)*

3. *(Canceled)*

4. *(Currently Amended)* A frequency divider as claimed in claim 1-2, wherein the control signal is a DC signal.

5. *(Currently Amended)* A frequency divider as claimed in claim 1-2, wherein the control signal is a complementary clock signal to the clock signal supplied to the first latch

6. *(Previously Presented)* A frequency divider as claimed in claim 5, wherein the first latch is substantially identical to the second latch

7. *(Currently Amended)* A frequency divider as claimed in claim 1-2, wherein each latch comprises a negative resistance coupled between the drains of said second transistor and said fourth transistor and between the drain of the fifth transistor and drain of the sixth transistor, respectively.

8. *(New)* A frequency divider comprising,  
a first latch comprising a clock input for receiving a clock signal, and  
a second latch comprising a latch circuit configured as a low-pass filter,  
the second latch being crossed-coupled to the first latch;  
wherein the second latch comprises  
a differential pair of transistors including  
a fifth transistor and a sixth transistor  
each transistor having a drain, a source and a gate,  
- a drain of the fifth transistor and the drain of the sixth transistor  
being coupled to supply voltage (Vs) via respective resistors,  
a source of the fifth transistor and a source of the sixth transistor  
being coupled to a common potential,  
gates of the fifth transistor and sixth transistor receiving a signal  
generated by the first latch.

9. *(New)* A frequency divider as claimed in claim 8, wherein the control signal is a DC signal.

10. *(New)* A frequency divider as claimed in claim 8, wherein the control signal is a complementary clock signal to the clock signal supplied to the first latch

11. *(New)* A frequency divider as claimed in claim 10, wherein the first latch is substantially identical to the second latch

12. *(New)* A frequency divider as claimed in claim 8, wherein each latch comprises a negative resistance coupled between the drains of said second transistor and said fourth transistor and between the drain of the fifth transistor and drain of the sixth transistor, respectively.